Arria® V Featured Documentation - Quick Links Guide

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Arria® V Featured Documentation - Quick Links

This page provides links to some of the key Arria® V documentation, organized by focused subject areas.

Featured Documents

Arria V FPGA Product Table	Device overview	Datasheet
Errata sheet	Arria V and Cyclone V Design Guidelines	Arria V and Cyclone V SoC Design Guidelines
Arria V Device Handbook: Volume 1: Device Interfaces and Integration	Arria V Device Handbook: Volume 2: Transceivers	Arria V Hard Processor System Technical Reference Manual
Package and Thermal specifications	Device pin-outs	Pin connection guidelines

See All Arria V Resources and Documentation

Device Handbook Sections

1. **Arria V Device Handbook: Volume 1: Device Interfaces and Integration**
   - **Section I. Device Core**
     - Chapter 1. Logic Array Blocks and Adaptive Logic Modules
     - Chapter 2. Embedded Memory Blocks
     - Chapter 3. Variable Precision DSP Blocks
     - Chapter 4. Clock Networks and PLLs
   - **Section II. I/O Interfaces**
     - Chapter 5. I/O Features
     - Chapter 6. High-Speed Differential I/O Interfaces and DPA
     - Chapter 7. External Memory Interfaces
   - **Section III. System Integration**
     - Chapter 8. Configuration, Design Security, and Remote System Upgrades
     - Chapter 9. SEU Mitigation
     - Chapter 10. JTAG Boundary-Scan Testing
     - Chapter 11. Power Management
2. **Volume 2 - Arria V Device Handbook: Transceivers**
   - Chapter 1. Transceiver Architecture
   - Chapter 2. Transceiver Clocking
   - Chapter 3. Transceiver Reset Control
   - Chapter 4. Transceiver Protocol Configurations

- Chapter 5. Transceiver Custom Configurations
- Chapter 6. Transceiver Configurations
- Chapter 7. Transceiver Loopback Support
- Chapter 8. Dynamic Reconfiguration

Power and Thermal Management

- PowerPlay Early Power Estimator User Guide
- Early Power Estimator Download for Arria II GX, Arria II GZ, and Arria V Devices
- Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide
- Power Delivery Network (PDN) Tool 2.0 for Stratix V, Arria V, Arria II GZ, Cyclone V, and Cyclone IV Devices
- AN 750: Using the Altera PDN Tool to Optimize Your Power Delivery Network Design

External Memory Interfaces

- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Introduction and Design Flow: For UniPHY-based Device Families
- External Memory Interface Handbook Volume 2: Design Guidelines: For UniPHY-based Device Families
- External Memory Interface Handbook Volume 3: Reference Material: For UniPHY-based Device Families

Design Guidelines

- Arria V and Cyclone V Design Guidelines
- AN 796: Cyclone V and Arria V SoC Device Design Guidelines
- Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines
- Arria V GZ Device Family Pin Connection Guidelines

Development Kits

- Arria V GX Starter Board Reference Manual
- Arria V GX FPGA Development Kit User Guide
- Arria V GX FPGA Development Board Reference Manual
- Arria V GT FPGA Development Board Reference Manual
- Arria V GT FPGA Development Kit User Guide
- Arria V SoC Development Board Reference Manual
- Arria V SoC Development Kit User Guide
- USB-Blaster Download Cable User Guide
- Arria V Boards

Hard Processor System (HPS)

- Arria V Hard Processor System Technical Reference Manual
- Arria V HPS Register Address Map and Definitions - Register Map
- AN 706: Routing HPS Peripheral Signals to the FPGA External Interface

Software Documentation

- Intel Quartus Prime Standard Edition User Guides - Combined PDF
- All Software Documentation

IP Documentation

- Advanced SEU Detection Intel FPGA IP User Guide
- ALTLVDS IP Core User Guide
- Arria V Avalon-MM Interface for PCIe Solutions: User Guide
- Arria V Avalon-ST Interface for PCIe Solutions: User Guide
- Arria V GZ Avalon-MM Interface for PCIe Solutions: User Guide
- Arria V GZ Avalon-ST Interface for PCIe Solutions: User Guide
- Arria V GZ Hard IP for PCIe User Guide
- Arria V Hard IP for PCIe User Guide
- CPRI Intel FPGA IP User Guide
- DisplayPort Intel FPGA IP User Guide
- Embedded Peripherals IP User Guide
- FIFO Intel FPGA IP User Guide
- JESD204B Intel FPGA IP User Guide
- Remote Update Intel FPGA IP User Guide
- Triple-Speed Ethernet Intel FPGA IP User Guide
- V-Series Transceiver PHY IP Core User Guide
- All Arria V Related IP Documentation

Application Notes

- AN668: Serial Digital Interface Reference Design for Stratix V GX and Arria V GX Devices
- AN 696: Using the JESD204B MegaCore Function in Arria V Devices
- Arria V Timing Optimization Guidelines
- Using the Transceiver Reconfiguration Controller for Dynamic Reconfiguration in Arria V and Cyclone V Devices
- All Arria V Related Application Notes